

Customer No.: 31561  
Docket No.: 12336-US-PA  
Application No.: 10/710,662

### REMARKS

#### Present Status of the Application

Claim 17 is objected to. The Office Action rejected claims 1-8, 10, 15, 16, 18 and 20 under 35 U.S.C. 102(b), as being anticipated by Chakravorty (US 6,181,569).

The dependency of claim 17 is amended to overcome the objection. Claims 1-8, 10, 15, 16, 18 and 20 remain pending in the present invention, and reconsideration of those claims is respectfully requested.

#### Claim Rejections under 35 U.S.C. 102(b)

*The Office Action rejected claims 1-8, 10, 15, 16, 18 and 20 under 35 U.S.C. 102(b) as being anticipated by Chakravorty. Applicant respectfully traverses the 102(b) rejection of claims 1-18 because Yu et al. does not teach each and every element recited in these claims.*

In order to properly anticipate Applicant's claimed invention under 35 U.S.C 102, each and every element of claim in issue must be found, "either expressly or inherently described, in a single prior art reference". "The identical invention must be shown in as complete details as is contained in the .... claim. Richardson v. Suzuki Motor Co., 868 F. 2d 1226, 1236, 9 USPQ2d

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1913, 1920 (Fed. Cir. 1989)." See M.P.E.P. 2131, 8<sup>th</sup> ed.,  
2001.

The present invention is related to a stress relieving method as amended claim 1 recites:

Claim 1. A stress relieving method for a wafer, comprising the steps of:

providing a wafer with a dielectric layer thereon, wherein the wafer is divided into  
a first area and a second area such that at least no circuits are formed on the dielectric layer  
within the first area;

*forming a plurality of first openings in the dielectric layer within the first area;*

and

forming a first material layer over the wafer, wherein the upper surface of the first  
material layer has pits at locations over the first openings, and the first material layer is a high  
stress dielectric layer.

Regarding to the rejection of claim 1, a telephone interview with the Examiner is conducted  
dated October 2, at 10:00 (ET). In the interview, we have discussed the Office Action dated  
08/08/2007 has selectively misconstrued the first area and the second area in Chakravorty. Even  
assuming that reference 304 of Chakravorty is comparable to the first area of the instant case,  
Chakravorty fails to teach forming a plurality of first openings within the first area where no  
circuits are formed on the dielectric layer within the first area since reference 304 itself is a metal  
contact pad and metal traces 307 are formed in the openings above reference 304. Moreover,

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Chakravorty definitely fails to teach or suggest "forming a first material layer over the wafer, wherein the upper surface of the first material layer has pits at locations over the first openings" since the pits 309 at the upper surface of the alleged first material layer 308 of Chakravorty are not at locations over the first openings above reference 304 in Figure 5.

The examiner has agreed that claim 1 define over Chakravorty.

In view of the foregoing or other reasons, Applicant respectfully submits independent claim 1 patentably defines over Chakravorty, and should be allowed. Since independent claim 1 should be allowed over the prior art of record, its dependent claims 2-8 should also be allowed as a matter of law, because the dependent claims contain all features of their respective independent claim 1.

The present invention is related to a stress relieving method as amended claim 10 recites:

Claim 10. A stress relieving method for a wafer, comprising the steps of:

providing a wafer with a dielectric layer thereon, wherein the wafer is divided into a first area and a second area such that no circuits are formed within the first area, *the first area comprising a scribe line, the second area comprising a region for forming a die, wherein there is no opening formed in the dielectric layer within the first area;*

forming a first material layer over the wafer to cover the dielectric layer; and

*forming a plurality of first openings in the first material layer within the first area.*

*(Emphasis added)*

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Applicant respectfully submits Chakravorty fails to teach forming a plurality of first openings in the first material layer within the first area comprising a scribe line as claim 10 recited. The office action stated Chakravorty disclosed the first area comprises a scribe line in Fig. 6. As a matter of fact, Fig. 6 is one of the steps for a chip package process, and the structure shown in Fig. 6 is in the region where the chip 302 is disposed. Please see Fig. 2 and col. 7, lines 45-47, Chakravorty disclosed the reference number 302 refers as a chip while the reference number 303 refers as a scribe line. In addition, the step shown in Fig. 6 is followed Figs. 4-5a, and the chip contact pads are labeled as reference number 304, and obviously, the chip contact pads in Fig. 6 is mis-labeled as reference number 303. Therefore, Fig. 6 of the citation does not show the scribe line, and thus Chakravorty does not teach the feature of forming a plurality of first openings in the first material layer within the first area comprising a scribe line.

In the telephone interview, we also discussed that the process step shown in Figure 6 follows those shown in Figures 4, 5 and 5a, in which the chip contact pads are labeled as reference number 304. Hence, it is obvious that the same elements (the chip contact pads) shown in Figure 6 are being mis-labeled as reference 303. As shown in Figure 2 and disclosed in col. 7, lines 45-47, Chakravorty discloses that the reference number 302 refers to a chip, while the reference number 303 refers to a scribe line. Figure 6 illustrates one of the steps of the chip package process and the structure shown in Figure 6 is in a region of a wafer where the chip 302 is disposed. Accordingly, Chakravorty does not teach the feature of forming a plurality of first openings in the first material within the first area comprising a scribe line.

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The examiner insists on further reviewing the prior art and recommends filing an argument with reference to claim 10.

In view of the foregoing or other reasons, Applicant respectfully submits Chakravorty fails to teach or suggest every element recited in claim 10. Therefore, Applicant respectfully submits that independent claim 10 patently defines over the prior art reference, and should be allowed. Since independent claim 10 should be allowed over the prior art of record, its dependent claims 15, 16-18 and 20 should also be allowed as a matter of law, because the dependent claims contain all features of their respective independent claim 10.

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**CONCLUSION**

For at least the foregoing reasons, it is believed that the pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

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Respectfully submitted,

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